WHAT IS CLAIMED IS:

1. A semiconductor device comprising;

a MOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate with intervention of a buried insulating film, and

a contact portion for applying to the semiconductor substrate different bias voltages in an operating state and a standby state of a semiconductor circuit including the MOS transistor.

2. A semiconductor device according to Claim 1, wherein the contact portion is formed on the semiconductor substrate.

3. A semiconductor device according to Claim 1, wherein an element isolating region is formed in the semiconductor layer, and a contact region is formed in the element isolating region for connection with the contact portion.

4. A semiconductor device according to Claim 1, wherein a well is formed in a surface of the semiconductor substrate which lies under the MOS transistor formed on the semiconductor layer, the well having an impurity concentration higher than that of the other region of the substrate, and the bias voltages are applied to the well.

5. A semiconductor device according to Claim 4, wherein the well is a P-type well under an N-channel MOS transistor, while the well is an N-type well under a P-channel MOS transistor.

6. A semiconductor device according to Claim 5, wherein a plurality of well are formed in the semiconductor substrate and the P-type well and the N-type well are electrically isolated from each other.

7. A semiconductor device comprising;

a MOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate with intervention of a buried insulating film,

an element isolating region formed in the semiconductor layer, and

a contact region formed in the element isolating region for connection with a contact portion for applying a bias voltage to the semiconductor substrate.

8. A semiconductor device according to Claim 7, wherein a well is formed in a surface of the semiconductor substrate which lies under the MOS transistor formed on the semiconductor layer, the well having an impurity concentration higher than that of the other region of the substrate, and the bias voltages are applied to the well.

9. A semiconductor device according to Claim 8, wherein the well is a P-type well under an N-channel MOS transistor, while the well is an N-type well under a P-channel MOS transistor.

10. A semiconductor device according to Claim 9, wherein a plurality of well are formed in the semiconductor substrate and the P-type well and the N-type well are electrically isolated from each other.

11. A semiconductor device according to Claim 7, wherein different bias voltages are applied in an operating state and a standby state of a semiconductor circuit including the MOS transistor, thereby to change a threshold voltage of the MOS transistor.

12. A semiconductor device comprising;

a MOS transistor formed on a second semiconductor layer of a

multilayer SOI substrate in which a first insulating layer, a first semiconductor layer, a second insulating layer and the second semiconductor layer are successively formed on a support substrate, and

a contact portion for applying a bias voltage to the first semiconductor layer.

13. A semiconductor device according to Claim 12, wherein the contact portion is formed on the semiconductor substrate.

14. A semiconductor device according to Claim 12, wherein an element isolating region is formed in the second semiconductor layer, and a contact region is formed in the element isolating region for connection with the contact portion.

15. A semiconductor device according to Claim 12, wherein a well is formed in a surface of the first semiconductor layer which lies under the MOS transistor formed on the second semiconductor layer, the well having an impurity concentration higher than that of the other region of the first semiconductor layer, and the bias voltage is applied to the well.

16. A semiconductor device according to Claim 15, wherein the well is a P-type well under an N-channel MOS transistor, while the well is an N-type well under a P-channel MOS transistor.

17. A semiconductor device according to Claim 16, wherein a plurality of well are formed in the semiconductor substrate and the P-type well and the N-type well are electrically isolated from each other.

18. A semiconductor device according to Claim 17, wherein the P-type well and the N-type well are electrically isolated by an insulating layer.

19. A semiconductor device according to Claim 18, wherein the insulating layer is part of an insulating layer which forms the element isolating region formed through the second semiconductor layer, the second insulating layer and the first semiconductor layer.

20. A semiconductor device according to Claim 12, wherein different bias voltages are applied in an operating state and a standby state of a semiconductor circuit including the MOS transistor, thereby to change a threshold voltage of the MOS transistor.

21. A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming an element isolating region in a surface semiconductor layer of an SOI substrate in which a buried insulating film and the surface semiconductor layer are formed on a semiconductor substrate or a semiconductor layer;

(b) forming in the element isolating region a trench which reaches the semiconductor substrate or the semiconductor layer;

(c) forming an insulating film on the whole area of the surface semiconductor layer which includes the trench;

(d) etching back the insulating film, thereby forming a side wall spacer on a side wall of the trench and exposing the semiconductor substrate or the semiconductor layer at a bottom of the trench; and

(e) burying a conductive film in the trench, thereby forming in the element isolating region a contact portion which is connected to the semiconductor substrate or the semiconductor layer.

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